# Lab 08 – Worksheet

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## Programming Basys-3 board

In this report, include following:

* Snapshot of simulation output of AND Gate.
* Add all codes related to adder subtractor
  + Design Modules
  + Constraint Files

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**Question 1**

**AND GATE**

**DESIGN FILE:**

module AND(

input A,

input B,

output C

);

assign C = A && B;

endmodule

**TESTBENCH:**

`timescale 1ns / 1ps

module Simulation();

reg A;

reg B;

wire C;

AND module\_u\_test (A, B,C);

initial begin

#100 A = 1'b0;

B = 1'b0;

#100 A = 1'b0;

B = 1'b1;

#100 A = 1'b1;

B = 1'b0;

#100 A = 1'b1;

B = 1'b1;

end

endmodule

**CONSTRAINT FILE:**

set\_property IOSTANDARD LVCMOS33 [get\_ports A]

set\_property IOSTANDARD LVCMOS33 [get\_ports B]

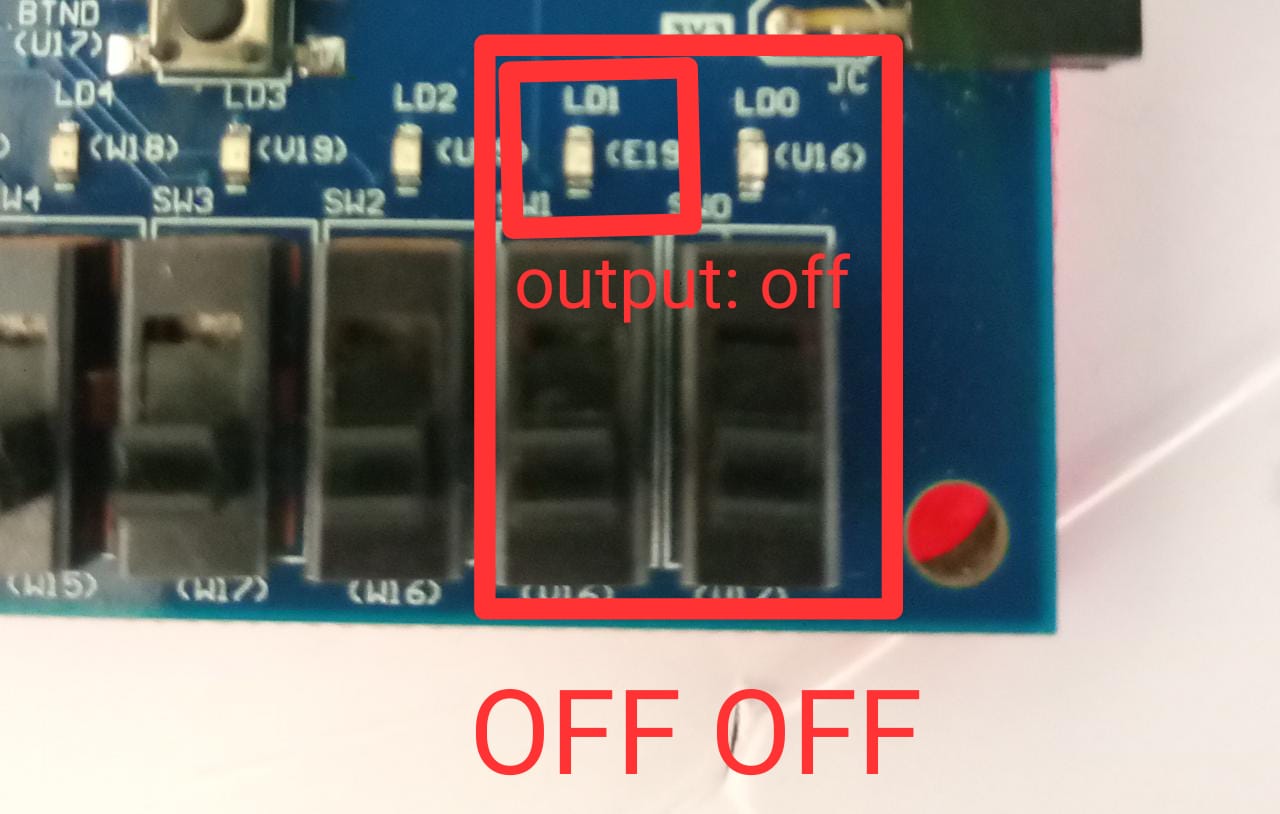
set\_property IOSTANDARD LVCMOS33 [get\_ports C]

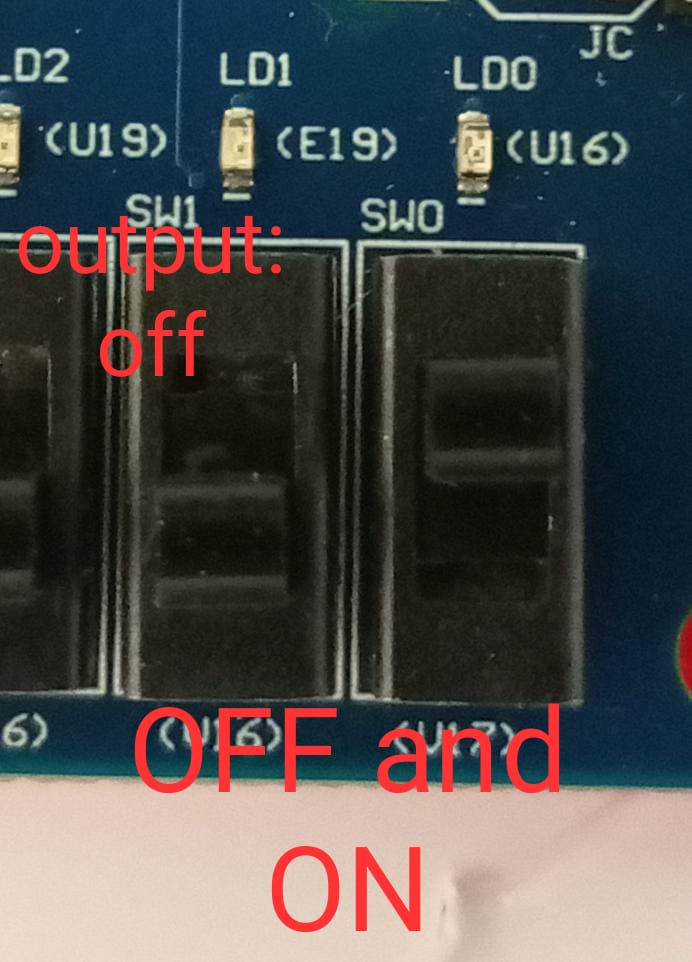
set\_property PACKAGE\_PIN V16 [get\_ports A]

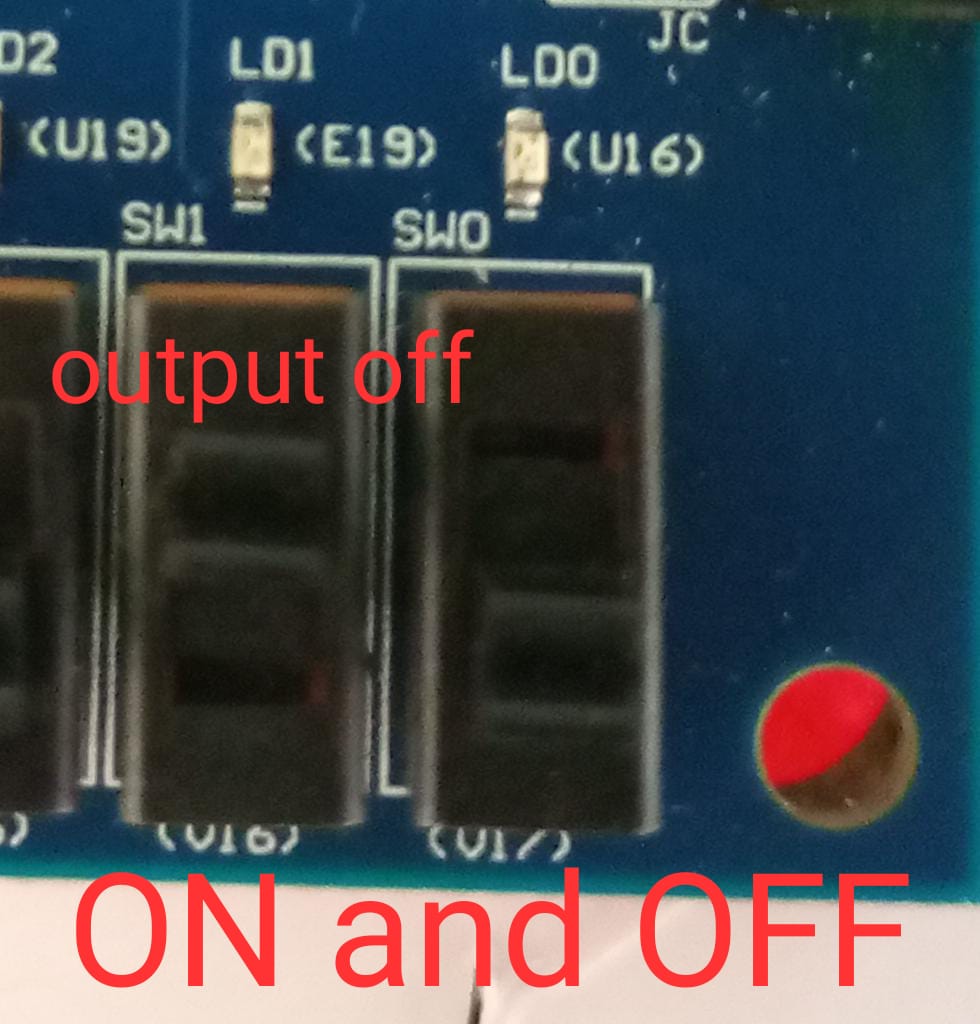
set\_property PACKAGE\_PIN V17 [get\_ports B]

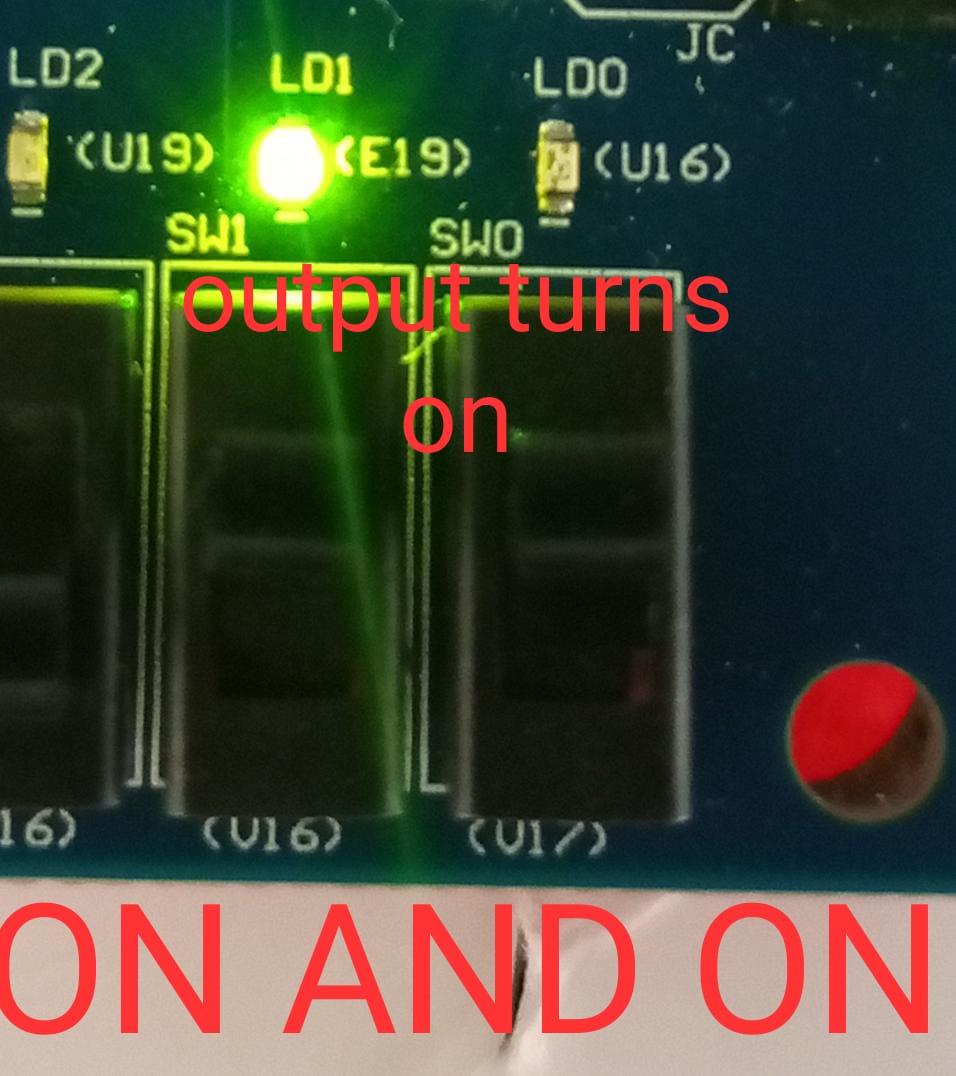
set\_property PACKAGE\_PIN E19 [get\_ports C]

**SIMULATION PICTURES:**

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**Question 2**

`timescale 1ns / 1ps

module Adder\_Subtractor\_3bit(

input [2:0] B,

input [2:0] A,

input O,

output [6:0] S,

output dp,

output [3:0] AN

);

wire [2:0] C;

SecondCompliment First\_Second (O, B[2:0], C[2:0]);

wire [3:0] U;

ThreeBitFullAdder TBFA( A [2:0], C [2:0], U [2:0], U[3]);

//underneath stuff.

wire Y, Y2, Y3, Y4;

not (Y, O);

//or-stuff

or (Y2,U[3],Y);

not(Y3,Y2);//Y3 selector bit for 2nd second compliment

wire [3:0] D;

and (Y4, U[3],Y);

assign D[3] = Y4;

//Y4 will go into 7 segment

SecondCompliment Second\_Second (Y3, U[2:0], D[2:0]);

SevenSegment SS (D[3:0] , S[6:0]);

assign dp = Y2;

assign AN[0]= 0 ;

assign AN[1]= 1 ;

assign AN[2]= 1 ;

assign AN[3]= 1 ;

endmodule

module SevenSegment(

input [3:0] D,

output [6:0] S);

assign S[0] = ((~D[3])&(~D[2])&(~D[1])&D[0]) | ((~D[3])&(D[2])&(~D[1])&(~D[0])) | ((D[3])&(~D[2])&(D[1])&D[0]) | ((D[3])&(D[2])&(D[1])&D[0]);

assign S[1] = ((D[2])&(D[1])&(~D[0])) | ((D[3])&(D[1])&(D[0])) | ((D[3])&(D[2])&(~D[0])) | ((~D[3])&(D[2])&(~D[1])&D[0]);

assign S[2] = ((D[3])&(D[2])&(~D[0])) | ((D[3])&(D[2])&(D[1])) | ((~D[3])&(~D[2])&(D[1])&(~D[0]));

assign S[3] = ((D[2])&(D[1])&D[0]) | ((~D[3])&(~D[2])&(~D[1])&(D[0])) | ((~D[3])&(D[2])&(~D[1])&(~D[0])) | ((D[3])&(~D[2])&(D[1])&(~D[0]));

assign S[4] = ((~D[3])&D[0]) | ((~D[2])&(~D[1])&(D[0])) | ((~D[3])&(D[2])&(~D[1]));

assign S[5] = ((~D[3])&(~D[2])&D[0]) | ((~D[3])&(~D[2])&(D[1])) | ((~D[3])&(D[1])&D[0]) | ((D[3])&(D[2])&(~D[1])&D[0]);

assign S[6] = ((~D[3])&(~D[2])&(~D[1])) | ((~D[3])&(D[2])&(D[1])&(D[0])) | ((D[3])&(D[2])&(~D[1])&(~D[0]));

endmodule

module SecondCompliment(

input O,

input [2:0] B,

output [2:0] C

);

assign C[2] = (((~O) & B[2]) | (B[2] & (~B[1]) & (~B[0])) | (O & (~B[2]) & B[0] | O & (~B[2]) & B[1]));

assign C[1] = (((~O)&B[1]) | (B[1] & (~B[0])) | (O & (~B[1])&B[0]));

assign C[0] = B[0];

endmodule

module Adder(

input a,

input b,

input c,

output sum,

output carry

);

wire x1,x2,x3;

xor(x1,a,b);

xor g2(sum,c,x1);

and(x2,c,x1);

and(x3,a,b);

or(carry,x2,x3);

endmodule

module ThreeBitFullAdder(

input [2:0] A,

input [2:0] B,

output [2:0] Y,

output Cout

);

wire [1:0] w1;

Adder add1(A[0],B[0],0,Y[0],w1[0]);

Adder add2(A[1],B[1],w1[0],Y[1],w1[1]);

Adder add3(A[2],B[2],w1[1],Y[2],Cout);

endmodule

///////////////////////////////////////////////////////////////////////////////

**//Constraint file**  
set\_property IOSTANDARD LVCMOS33 [get\_ports {A[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {A[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {A[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {B[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {B[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {B[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {S[6]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {S[5]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {S[4]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {S[3]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {S[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {S[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {S[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports dp]

set\_property IOSTANDARD LVCMOS33 [get\_ports O]

set\_property PACKAGE\_PIN W7 [get\_ports {S[0]}]

set\_property PACKAGE\_PIN W6 [get\_ports {S[1]}]

set\_property PACKAGE\_PIN U8 [get\_ports {S[2]}]

set\_property PACKAGE\_PIN V8 [get\_ports {S[3]}]

set\_property PACKAGE\_PIN U5 [get\_ports {S[4]}]

set\_property PACKAGE\_PIN V5 [get\_ports {S[5]}]

set\_property PACKAGE\_PIN U7 [get\_ports {S[6]}]

set\_property PACKAGE\_PIN V7 [get\_ports dp]

set\_property PACKAGE\_PIN W17 [get\_ports O]

set\_property PACKAGE\_PIN W14 [get\_ports {A[2]}]

set\_property PACKAGE\_PIN V15 [get\_ports {A[1]}]

set\_property PACKAGE\_PIN W15 [get\_ports {A[0]}]

set\_property PACKAGE\_PIN W16 [get\_ports {B[2]}]

set\_property PACKAGE\_PIN V16 [get\_ports {B[1]}]

set\_property PACKAGE\_PIN V17 [get\_ports {B[0]}]

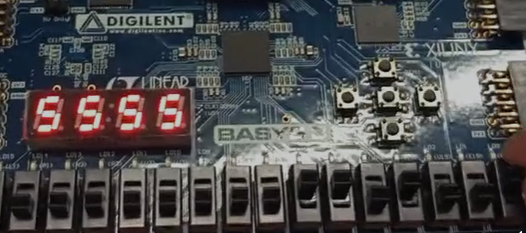
**//Simulation pictures:**

*Note: I forgot to take pictures of the simulation as I thought the question asked for topLevelModule Simulation. However, I did make a video of my working FPGA. Screenshots from that video are attached, I apologize for the potential blurriness.*

Test Case 1:  
6+0 =6



Test Case 2:  
6-1 = 5

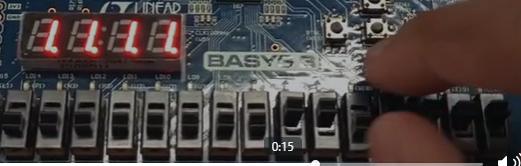


Test Case 3:  
7+7 = E



Test Case 4:

6-7 = -1 (represented with a dot)



**Assessment Rubrics**

**Marks Distribution:**

|  |  | **LR2**  **Code/Simulation (In-Lab)** | **LR5**  **Results** | **LR7**  **Viva** | **LR9**  **Report** |
| --- | --- | --- | --- | --- | --- |
| **In-lab** | **Task b** | - | 10 points | 10 points | 10 points |
| **Task c** | - | 10 points |
| **Task d** | 20 points | 10 points | 30 points |
| **Total marks 100** |  | 20 | 50 | 10 | 40 |

**Marks Obtained:**

|  |  | **LR2**  **Code/Simulation (In-Lab)** | **LR5**  **Results** | **LR7**  **Viva** | **LR9**  **Report** |
| --- | --- | --- | --- | --- | --- |
| **In-lab** | **Task b** | - |  |  |  |
| **Task c** | - |  |
| **Task d** |  |  |  |
| **Total marks 100** |  |  |  |  |  |